REMARKS

Applicant has considered the Office Action dated January 4, 2009, and the references cited therein. Claims 1-11, 13 and 15-17 are currently pending. No claims presently stand allowed.

Applicant has amended claim 17 to address the Section 112, written description, rejection at page 2 of the Office Action.

Applicant traverses the prior art-based rejections of the pending claims for the reasons set forth herein below.

Applicant requests favorable reconsideration of the Office Action's grounds for rejecting the previously pending claims in view of Applicant's amendments to the previously pending claims and the Remarks provided herein below.

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Summary of the Rejections

1. Claim 17 is rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

2. Claims 1-3, 5-7, 9, 13 and 15-17 are rejected under 35 U.S.C. §103(a) as obvious over Cohen et al. U.S. Patent No. 5,115,506 (Cohen).

3. Claim 4 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of Petolino, Jr., et al. U.S. Patent No. 5,958,041 (Petolino).

4. Claim 8 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of Patterson et al., "Computer Organization & Design: The Hardware/Software Interface"(Patterson).

5. Claim 10 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of Nguyen et al. U.S. Patent No. 5,448,705 (Nguyen).

6. Claim 11 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of Lang et al., "Individual Flip-Flops with Gated Clocks for Low Power Datapaths"(Lang).

Applicant traverses the grounds for each and every rejection for at least the reasons set forth herein below. Applicant addresses the specific rejections in the order they arise in the Office Action.

1. *Rejection of Claim 17 under §112, first paragraph, as failing to comply with the written description requirement*

Applicant traverses the rejection of claim 17 as failing to comply with the written description requirement. The Office Action states that the application, at the time of filing, did not disclose the recited *saving state information* to the snapshot buffer.

Applicants note that the Final Office Action did not address this portion of claim 17. In particular, the Final Office Action stated:

> "This disclosure teaches nothing regarding addressing snapshot buffer elements without using any instruction bits, but rather only teaches that certain commands do not require a register address. There is no mention in this teaching of addressing of snapshot buffer elements, with or without instruction bits."

See, Final Office Action, page 3 (bottom). Applicant respectfully noted that paragraph 19, lines 5-6, of Applicant's published application states:

> "Hence, no additional instruction bits will be required for addressing the registers in the snapshot buffer."

Notwithstanding the belief that claim 17 was supported by the written description, Applicant has further amended claim 17 to clarify the meaning of the claim.

Regarding the grounds (in the current Office Action) for rejecting claim 17 as lacking written description support with regard to "saving state information" to the snapshot buffer, Applicants note that the saving of state information (during an interrupt) to the snapshot buffer is the focus of the disclosed invention (*see*, Abstract) and the entire disclosure. Written description support for the claimed saving of state information to the snapshot buffer is provided, for example, in the paragraphs that proceed paragraph 19 of Applicant's published application. *See,*

e.g., paragraph 16, lines 11-16. Thus, the content of paragraphs 16-19 of Applicants' published application provides written description support for the recited elements of claim 17 relating to the storing of processor element state information in a snapshot buffer.

2. Rejection of Claims 1-3, 5-7, 9, 13 and 15-17 as Obvious Over Cohen

Applicant traverses the obviousness rejection of independent **claim 1** and claims 2, 3, 5-7, 9, 13 and 15-17, which depend from claim 1. The Cohen reference, upon which the obviousness rejection of claim 1 solely relies, neither discloses nor suggests at least one recited element (e.g., snapshot buffer "differing from the one or more register files") in claim 1. Applicant, addressing the "Response to Arguments" at page 11 of the Office Action, has amended claim 1 to make clear that an actual transfer of state information occurs *from the register files to the snapshot buffer elements during interrupt handling*. Thus, a *prima facie* case of obviousness has not been established. Furthermore, as noted in Applicant's previous response, where differences exist between Applicant's claimed invention and Cohen, the cited Cohen reference *teaches away from the claimed invention*. Thus, the claimed invention would not have been obvious to one skilled in the art at the time of the invention in view of Cohen's teachings.

Applicant's Claimed Invention

Applicant's claim 1 recites a data processor including one or more functional units, one or more register files, a data memory, and a snapshot buffer. During handling of an interrupt condition, the snapshot buffer accommodates saving state information of various processor state elements, including state information from the internal processor pipeline formed by the functional units. The claimed data processor includes "controller means" (see controller 26) that, upon entry of an interrupt processing state, save the state information of processor state elements (registers) currently within the snapshot buffer in the data memory facility having the multibit access port facility.

Thus, regarding the invention recited in amended (making clear that state information is transferred from the register files to the distinct memory of the snapshot buffer) claim 1, the snapshot buffer differs from the claimed register files and is provided *in addition to* the set of

one or more register files. As a consequence, during handling of an interrupt the snapshot buffer receives/saves state information of various processor state elements (registers). The state information stored in the snapshot buffer includes state information from the internal processor pipeline. During handling of an interrupt condition, information from processor state elements is transferred to the snapshot buffer elements. Furthermore, upon issuance of a subsequent interrupt during processing of a current interrupt, the contents of the snapshot buffer elements are transferred to the "data memory facility having the multibit port facility" (to make room in the snapshot buffer for the state information from the internal processor pipeline).

Cohen's Disclosure

Cohen discloses a microprocessor (10) including:

a. unprimed registers (20) used during normal processor operation,

b. prime registers (22) used during interrupts,

c. a normal register set (16) used during normal processor operation and conventional interrupt operation,

d. an alternate register set (18) for use during fast interrupt operations, and

e. a memory stack (50).

During normal operation the processor state information (SR, CSC, PC) is stored in the set of unprimed registers. During an interrupt the processor state information *is not saved to a "snapshot buffer"* as described/claimed by Applicant. Instead, Cohen discloses that when an initial interrupt arises, the CPU ceases using the unprimed registers and commences using the prime registers. *See,* Cohen, col. 4, lines 28-33. If a subsequent interrupt arises before the microprocessor completes processing a previous interrupt, the current contents of the prime registers are pushed onto the memory stack, and the processor processes the interrupt using the new information (associated with the subsequent interrupt) stored in the prime registers.

Thus, the microprocessor structure disclosed in Cohen must choose between two register banks (unprimed and primed) when state information is required. This requirement/limitation of Cohen is particularly problematic with regard to the program counter (PC) register, which must

be read by the processor during each processor cycle. The decision regarding which register bank to use (to access the PC value) injects a delay in a critical processing sequence regardless of whether the microprocessor is operating in a normal or interrupt mode. The need to choose between normal and interrupt register sets extends as well to reading operand information.

Non-Obvious Differences Between Cohen and Applicant's Claimed Invention

In accordance with the claimed invention, the functional units access the same state elements (registers) without regard to whether the processor is currently operating in a normal or interrupt mode. Rather than "switching" (per Cohen's explicit teachings) between two sets of registers (in accordance with normal/interrupt modes of operation of the processor) the claimed invention recites the "snapshot buffer" including a set of elements (registers) for receiving the current state information of the internal processing pipeline. According to Applicant's claimed invention, when a nested (subsequent) interrupt occurs during processing of a current interrupt, the contents of the snapshot buffer are transferred to the data memory facility including the multibit access port facility to enable updating the snapshot buffer with the current processor state information. Thus, at any point in time, regardless of the normal/interrupt state of Applicant's claimed processor, the functional units continuously access a same set of processor state elements (registers).

Cohen's explicit and unequivocal disclosure of *switching* between two distinct sets of registers (primed and unprimed) containing state information *teaches away from* Applicant's claimed invention wherein state information is transferred to a snapshot buffer when an interrupt occurs (to make room for new state information associated with a current interrupt operational mode of the processor), and thus a *same* set of registers are accessed by the functional units to access state information without regard to the normal/interrupt status of the processor. For at least this reason, the claimed invention is not rendered obvious by the teachings of Cohen.

Applicant's amendments have addressed a perceived lack of specificity noted in the Office Action with regard to whether state information is actually transferred from register files to the claimed snapshot buffer elements. The current amendments unequivocally resolve this potential ambiguity – i.e., there is an actual transfer between the two distinct sets of memory

elements. Therefore, in the event that the rejection of claim 1 is not withdrawn, Applicant respectfully requests identification of particularized teachings in the prior art disclosing the missing elements (e.g., snapshot buffer) of Cohen as well as a basis for modifying the unequivocal teachings of Cohen to render Applicant's claimed invention.

Claims **2, 3, 5-7, 9, 13 and 15-17** are dependent from claim 1, and therefore Applicant respectfully submits that these claims are not rendered obvious by Cohen for at least the reason that each of the dependent claims (from independent claim 1) includes at least one element that is not disclosed or suggested in Cohen in view of the state of the art.

3. Rejection of Claims 4, 8, 10 and 11 as being obvious over Cohen in view of various prior art references (i.e., Petolino, Patterson, Nguyen, Lang, and Kleiman

Claim 1 is not rendered obvious by Cohen at least because Cohen does not disclose or suggest the above-identified/discussed missing claim elements. The identified missing claim elements are also not disclosed or suggested by the various secondary references cited in the Office Action in support of the rejections of **claims 4, 8, 10 and 11**. Therefore, Applicant respectfully submits that claims 4, 8, 10 and 11, are not rendered obvious by the identified combinations of prior art references. Applicant notes that claim 12 has been canceled without prejudice.

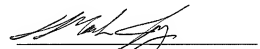
Applicant furthermore notes, again, with respect to the rejection of **claim 10**, Nguyen discloses, at column 3, lines 58-61 that "Register contents are not transferred; rather, the shadow registers are simply made available in place of the normal registers." Thus, Nguyen, like Cohen, teaches *switching* between two sets of registers, while the claimed invention recites *copying contents of state information registers* to a snapshot buffer when an interrupt occurs. As explained by Applicant previously herein above, copying contents of a register to a snapshot buffer differs substantially from Nguyen and Cohen's disclosed switching/replacing the location of state information registers when a processor enters an interrupt processing state.

In view of the above reasons, Applicant respectfully submits that claim 10 is not obvious over Cohen in view of Nguyen.

Conclusion

Applicant respectfully submits that the patent application is in condition for allowance. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,



Mark Joy, Reg. No. 35,562
LEYDIG, VOIT & MAYER, LTD.
Two Prudential Plaza, Suite 4900
180 North Stetson Avenue
Chicago, Illinois 60601-6731
(312) 616-5600 (telephone)
(312) 616-5700 (facsimile)

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